

What is claimed is:

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- 1 1. A system comprising:
2 a storage element;
3 a memory hierarchy coupled to the storage element;
4 a processor coupled to the memory hierarchy, wherein the processor executes
5 instructions from the memory hierarchy and a replay handler is loaded into the memory
6 hierarchy and the processor executes the replay handler for replaying at least one
7 execution.
 - 1 2. The system of claim 1 wherein the memory hierarchy is an instruction cache.
 - 1 3. The system of claim 1 wherein the the replay handler is loaded into the memory
2 hierarchy in response to a signal.
 - 1 4. The system of claim 1 wherein the replay handler includes the at least on
2 execution.
 - 1 5. The system of claim 1 wherein the replay handler loads the at least one
2 execution into the memory hierarchy from an external device.
 - 1 6. A system for replaying executions comprising:
2 a storage element;
3 a memory hierarchy coupled to the storage element;
4 a system bus coupled to the memory hierarchy;
5 a processor coupled to the system bus, wherein the processor executes instructions from
6 the memory hierarchy and wherein on a break, the processor reaches a steady state,
7 transfers original code of the memory hierarchy to the storage element, loads a replay
8 handler into the memory hierarchy and the processor executes the replay handler to
9 replay at least one execution.

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- 1 7. The system of claim 6 wherein the original code is loaded into the memory
2 hierarchy after the at least one execution has been replayed.
- 1 8. The system of claim 6 further comprising a system memory and wherein the
2 storage element is a location in the system memory.
- 1 9. The system of claim 6 wherein the storage element is a hard drive.
- 1 10. A system comprising:
2 a memory hierarchy;
3 a processor coupled to the memory hierarchy wherein the processor executes
4 instructions from the memory hierarchy;
5 a port coupled to the processor and memory hierarchy;
6 a host system coupled to the port; and
7 wherein the host system generates a replay handler, generates at least one
8 execution and generates a signal for replaying the at least one execution.
- 1 11. The system of claim 10 wherein on the signal, original code of the memory
2 hierarchy is saved, the replay handler is loaded into the memory hierarchy from the host
3 system through the port, and the replay handler is executed by the processor.
- 1 12. The system of claim 11 wherein on the replay handler being executed, the replay
2 handler is modifiable by the host system.
- 1 13. The system of claim 12 wherein the replay handler is modified to alter starting
2 and stopping points of one of the at least one executions.
- 1 14. The system of claim 10 wherein a replay state is sent to the host system through
2 the port.

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- 1 15. The system of claim 10, wherein the port is a network interface.
- 1 16. The system of claim 10, wherein the port is a serial interface.
- 1 17. A method for replaying executions comprising:
2 interrupting normal processor execution;
3 loading a replay/restart kernel;
4 replaying at least one execution; and
5 resuming normal executions.
- 1 18. The method of claim 17 further comprising generating the at least one execution.
- 1 19. The method of claim 18 further comprising accessing state information.
- 1 20. A method comprising:
2 interrupting processes executing on a processor;
3 storing minimal state information sufficient to later resume the interrupted
4 processes;
5 storing original code of an instruction cache;
6 loading a replay handler into the instruction cache;
7 branching execution of the processor to the replay handler;
8 replaying a system execution a number of times from a starting point to a
9 stopping point while monitoring state information;
10 loading the original code into the instruction cache; and
11 resuming interrupted processes utilizing the minimal state information.
- 1 21. The method of claim 20 further comprising:
2 modifying the number of times, the starting point and the stopping point by a
3 user.

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